IN THE DRAWINGS:

Amended Figure 3A in one sheet of drawing is submitted herewith.

IN THE SPECIFICATION:

Page 5, lines 11-12, change "in the controller" to --on a Flash EEprom chip--.

IN THE CLAIMS:

Cancel non-elected claims 1-29 and 56-62.

Cancel claims 34, 40, 48, and 54

Amend claims 30-33, 35-39, 41-47, 49-53 and 55 as follows:

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30. (Amended) An improved [system for writing data files into a Flash EEprom memory] Flash EEprom system with reduced write-related stress, comprising:

a Flash EEprom memory for storing data files from a host system;

a cache memory for temporarily storing data files intended for the Flash Eeprom memory, said cache memory able to undergo significantly more write/erase cycles than the Flash Eeprom memory;

[means responsive to a system write to the Flash EEprom memory] a controller for controlling memory operations in said Flash EEprom memory and said cache memory; said controller responsive to a write request from the host system for writing data files into the cache memory instead of the Flash EEprom memory;

[means for identifying each data file in the cache memory;]

timing means for determining the time since each data file was last written into said cache memory; and

written from the cache memory to the Flash EEprom memory when additional space for new data files is required in the cache memory, thereby substantially reducing the number of actual writes and associated stress to the Flash EEprom memory.

31. (Amended) The improved Flash EEprom system as in claim 30, further comprising:

a backup non-volatile memory for downloading the data files in the cache memory thereto; and

[means responsive to an impending power loss] said controller responsive to a power loss in the host system for down loading the data files in the cache memory to the backup memory, thereby saving the data files from the possibly volatile cache memory.

32. (Amended) The improved Flash EEprom system as in claim [30] 31, wherein the backup memory is part of the Flash EEprom memory.

33. (Amended) The improved Flash EEprom system as in claim 30, wherein the cache memory has a significantly faster access time than that of the Flash EEprom memory.

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34. (Canceled) The improved system as in claim 30, including a controller circuit chip for controlling the operations of the Flash EEprom memory, wherein the improved system is part of the controller circuit chip.

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35. (Amended) The improved Flash EEprom system as in claim 30, [including] wherein said host system includes a microprocessor system and random access memory, [wherein the improved system is implemented] and said cache memory is part of

36. (Amended) An improved [system for writing data files into a Flash EEprom memory] Flash EEprom system with reduced write-related stress, comprising:

a Flash EEprom memory for storing data files from a host system;

a cache memory for temporarily storing data files intended for the Flash EEprom memory, said cache memory able to undergo significantly more write/erase cycles than the Flash EEprom memory;

[means responsive to a system write to the Flash EEprom memory] a controller for controlling memory operations in said Flash EEprom memory and said cache memory; said controller responsive to a write request from the host system for writing data files into the cache memory instead of the Flash EEprom memory;

[means for identifying each data file in the cache memory;]

a tag memory for storing the identity of data files and the time each data file was last written into said cache memory; and

[means for] said controller in reference to said tag memory first moving a data file having the longest time since last written from the cache memory to the Flash EEprom memory when additional space for new data files is required in the cache memory, thereby substantially reducing the number of actual writes and associated stress to the Flash EEprom memory.

37. (Amended) The improved Flash EEprom system as in claim 36, further comprising:

a backup non-volatile memory for downloading the data files in the cache memory thereto; and

[means responsive to an impending power loss] said controller responsive to a power loss in the host system for down

thereby saving the data files from the possibly volatile cache memory.

38. (Amended) The improved Flash EEprom system as in claim [36] 37, wherein the backup memory is part of the Flash EEprom memory.

39. (Amended) The improved Flash EEprom system as in claim 36, wherein the cache memory has a significantly faster access time than that of the Flash EEprom memory.

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40. (Canceled) The improved system as in claim 36, including a controller circuit chip for controlling the operations of the Flash EEprom memory, wherein the improved system is part of the controller circuit chip.

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41. (Amended) The improved Flash EEprom system as in claim 36, [including] wherein said host system includes a microprocessor system and random access memory, [wherein the improved system is implemented] and said cache memory and said tag memory are part of the random access memory and said controller is controlled by software in the microprocessor system.

42. (Amended) An improved [system for writing data files into a Flash EEprom memory] Flash EEprom system with reduced write-related stress, comprising:

a Flash EEprom memory for storing data files from a host system;

a cache memory for temporarily storing data files intended for the Flash EEprom memory, said cache memory able to undergo significantly more write/erase cycles than the Flash EEprom memory;

Flash EEprom memory and said cache memory; said controller responsive to a write request from the host system for writing a data file either into the Flash EEprom memory [or instead into the cache memory, said responsive means writing to the Flash EEprom] when [the] a previous copy of said data file is not present in the cache memory, [and writing to] or into the cache memory when a previous copy of said data file is present in the cache memory; and

[means for] said controller first moving a data file having the longest time since last written from the cache memory to the Flash EEprom memory when additional space for new data files is required in the cache memory, thereby substantially reducing the number of actual writes and associated stress to the Flash EEprom memory.

43. (Amended) The improved Flash EEprom system as in claim 42, further comprising:

a backup non-volatile memory for downloading the data files in the cache memory thereto; and

[means responsive to an impending power loss] said controller responsive a power loss in the host system for down loading the data files in the cache memory to the backup memory, thereby saving the data files from the possibly volatile cache memory.

44. (Amended) The improved Flash EEprom system as in claim [42] 43, wherein the backup memory is part of the Flash EEprom memory.

45. (Amended) The improved Flash EEprom system for writing data files into a Flash EEprom memory according to claim 42, [wherein said responsive means for writing includes] further including a tag memory for storing the identity of data files and

EEprom when said data file is not tagged in the tag memory, and writing to the cache memory when said data file is tagged in the tag memory.

46. (Amended) An improved [system for writing data files into a Flash EEprom memory] Flash EEprom system with reduced write-related stress, comprising:

a Flash EEprom memory for storing data files from a host system;

a cache memory for temporarily storing data files intended for the Flash EEprom memory, said cache memory able to undergo significantly more write/erase cycles than the Flash EEprom memory;

[means responsive to a system write to the Flash EEprom memory] a controller for controlling memory operations in said Flash EEprom memory and said cache memory; said controller responsive to a write request from the host system for writing a data file either into the Flash EEprom memory [or instead into the cache memory, said responsive means writing to the Flash EEprom] when said data file is last written after [the] a predetermined period of time, [and writing to] or into the cache memory when said data file is last written within [a] the predetermined period of time; and

[means for] said controller first moving data file having the longest time since last written from the cache memory to the Flash EEprom memory when additional space for new data files is required in the cache memory, thereby substantially reducing the number of actual writes and associated stress to the Flash EEprom memory.

47. (Amended) The improved Flash EEprom system as in claim 46, wherein the cache memory has a significantly faster

48. (Canceled) The improved system as in claim 46, including a controller circuit chip for controlling the operations of the Flash EEprom memory, wherein the improved system is part of the controller circuit chip.

49. (Amended) The improved Flash EEprom system as in claim 46, [including] wherein said host system includes a microprocessor system and random access memory, [wherein the improved system is implemented] and said cache memory is part of the random access memory and said controller is controlled by software in the microprocessor system.

50. (Amended) An improved [system for writing data files into a Flash EEprom memory] Flash EEprom system with reduced write-related stress, comprising:

a Flash EEprom memory for storing data files from a host system;

a cache memory for temporarily storing data files intended for the Flash EEprom memory, said cache memory able to undergo significantly more write/erase cycles than the Flash EEprom memory;

a tag memory for storing the identity of data files and the time each data file was last written into said cache memory;

[means responsive to a system write to the Flash EEprom memory] a controller for controlling memory operations in said Flash EEprom memory and said cache memory; said controller responsive to a write request from the host system for writing a data file either into the Flash EEprom memory [or instead into the cache memory, said responsive means writing to the Flash EEprom] when the data file is not identified in the tag memory, [and writing to] or into the cache memory when the data file is identified in the tag memory; and

last written from the cache memory to the Flash EEprom memory when additional space for new data files is required in the cache memory, thereby substantially reducing the number of actual writes and associated stress to the Flash EEprom memory.

51. (Amended) The improved Flash EEprom system as in claim 50, further comprising:

a backup non-volatile memory for downloading the data files in the cache memory thereto; and

[means responsive] said controller responsive to [an impending power loss] a power loss in the host system for down loading the data files in the cache memory to the backup memory, thereby saving the data files from the possibly volatile cache memory.

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52. (Amended) The improved Flash EEprom system as in claim [50] 51, wherein the backup memory is part of the Flash EEprom memory.

53. (Amended) The improved Flash EEprom system as in claim 50, wherein the cache memory has a significantly faster access time than that of the Flash EEprom memory.

54. (Canceled) The improved Flash EEprom system as in claim 50, including a controller circuit chip for controlling the operations of the Flash EEprom memory, wherein [the improved] said cache system is part of the controller circuit chip.

55. (Amended) The improved Flash EEprom system as in claim 50, [including] wherein said host system includes a microprocessor system and random access memory, [wherein the improved system is implemented] and said cache memory and said tag

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Please add new claims 63-67 as follows:

--63. (New) A method for extending the life of Flash EEprom memory in a Flash EEprom system, comprising the steps of:

temporarily storing data files from a host system intended for the Flash EEprom memory in a cache memory, said cache memory able to undergo significantly more write/erase cycles than the Flash EEprom memory;

writing data files into the cache memory instead of the Flash EEprom memory in response to a write request from the host system;

determining the time since each data file was last written into said cache memory; and

moving first a data file having the longest time since last written first from the cache memory to the Flash EEprom memory when additional space for new data files is required in the cache memory, thereby substantially reducing the number of actual writes and associated stress to the Flash EEprom memory.--

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--64. (New) A method for extending the life of Flash EEprom memory in a Flash EEprom system, comprising the steps of:

temporarily storing data files from a host system intended for the Flash EEprom memory in a cache memory, said cache memory able to undergo significantly more write/erase cycles than the Flash EEprom memory;

writing data files into the cache memory instead of the Flash EEprom memory in response to a write request from the host system;

storing the identity of data files and the time each data file was last written into said cache memory in a tag memory; and

by reference to the tag memory, moving data file having the longest time since last written first from the cache memory to

number of actual writes and associated stress to the Flash EEprom memory.--

--65. (New) A method for extending the life of Flash EEprom memory in a Flash EEprom system, comprising the steps of:

temporarily storing data files from a host system intended for the Flash EEprom memory in a cache memory, said cache memory able to undergo significantly more write/erase cycles than the Flash EEprom memory;

in response to a write request from the host system, writing a data file either into the Flash EEprom memory when a previous copy of said data file is not present in the cache memory, or into the cache memory when a previous copy of said data file is present in the cache memory; and

moving data file having the longest time since last written first from the cache memory to the Flash EEprom memory when additional space for new data files is required in the cache memory, thereby substantially reducing the number of actual writes and associated stress to the Flash EEprom memory.--

--66. (New) A method for extending the life of Flash EEprom memory in a Flash EEprom system, comprising the steps of:

temporarily storing data files from a host system intended for the Flash EEprom memory in a cache memory, said cache memory able to undergo significantly more write/erase cycles than the Flash EEprom memory;

in response to a write request from the host system, writing a data file either into the Flash EEprom memory when said data file is last written after a predetermined period of time, or into the cache memory when said data file is last written within the predetermined period of time; and

moving data file having the longest time since last